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IMPLEMENTATION OF THE MAC UNIT OF 64 BIT HIGH PERFORMANCE SYSTEMS

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ABSTRACT:

Here the analysis of the system under which it includes the design based specification of the implementation of the accumulator and the multiplier of the 64 bit standard under which it is implemented in a well effective standard under which the design includes the standards of the improved performance plays a crucial role in its analysis based perspective respectively. Here the performance of the unit under the strategy of the MAC is a major concern under the applicability of the DSP based operations and the following standards respectively. Here the complete well effective design of the multiplier under which it is implemented with respect to the modification of the multiplier under the well effective strategy of the Wallace plays a major role and the adder of the carry save is mainly used for the purpose of the adding of the data or even the summing of the data in the carry save basis respectively. Here the coding of the complete design plays a crucial role in its analysis based perspective which includes the specification of the HDL oriented verilog and in a well effective manner followed by the integrity of the complete data oriented synthesis is done with respect to the analysis based perspective under the compilation of the RTL based cadence plays a crucial and the well effective role by the integration of the technology of the 0.18 micro meter TSMC and the standards of the typical libraries plays a crucial role in its implementation based perspective respectively. Here the complete operation of the unit of the MAC is done under the frequency of the 217 mega hertz in an analogous fashion with respect to the design based standards of the dissipation of the power is restricted

to the 177.32mag watt respectively. Experiments have been conducted on the present method where there is a lot of analysis under which a large number of the test bed is conducted with the variation in the data in terms of the unknown environments for the study of the effectiveness of the present method in a well effective and the efficient manner respectively.

KEYWORDS: Unit of MAC, Accumulator and the followed by the multiplier, Process of the digital signal, Logic of the real time strategy, Logic of the hardware description, Adder of the carry save, Multiplier of the modified Wallace respectively.

1. INTRODUCTION:

Here in terms of the applications of the processing of the data in the digitized fashion is playing a crucial role in its analysis based perspective in a well oriented fashion for the rapid advancement of the operation of the data in terms of the complexity of the operation of the addition followed by the multiplication is a major concern respectively [1]. Here in terms of the typical applicability of the operations related to the MAC based strategy there is an effective integration of the protocol of the MAC plays a well efficient and the effective role in its synthesis followed by the operation based perspective respectively. Here for the purpose of the improvement of the performance of the system in a well effective fashion by the help of the integration of the design oriented protocol of the MAC layer is a major concern respectively. Here some of the applications of the processing of the data in the digitized fashion includes the convolution, correlation and followed by the filtering is a major concern respectively. Here for the applications based perspective there is a utilization of the functions of the non linear basis apart from the linear standards and some of them includes the transformation of the discrete cosine data followed by the discrete wavelet based strategy in terms of the analysis and the data representation is a major concern respectively [2][3]. Here these particular analysis based applications are well effective in terms of the implementation of the system and for the improvement in the performance based standards of the entire system in a stipulated fashion respectively.

BLOCK DIAGRAM

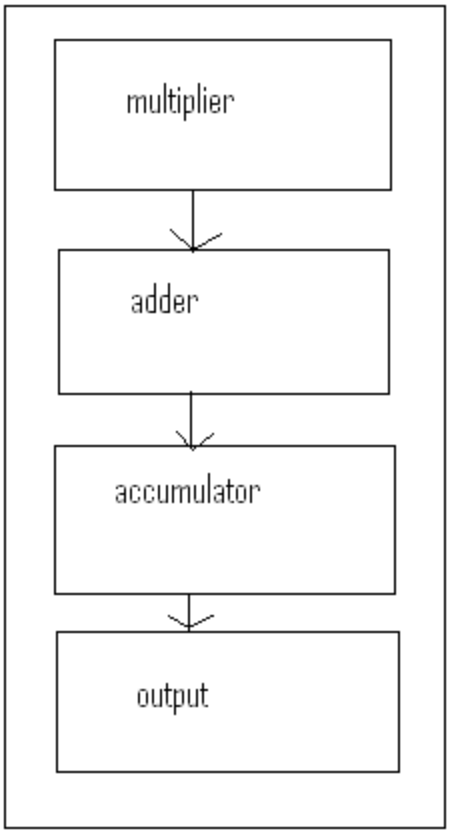


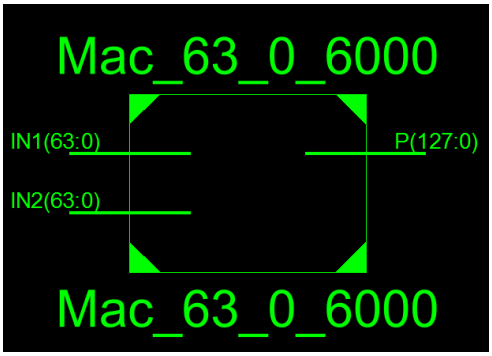
Figure shows the block diagram of the present method respectively

2. METHODOLOGY:

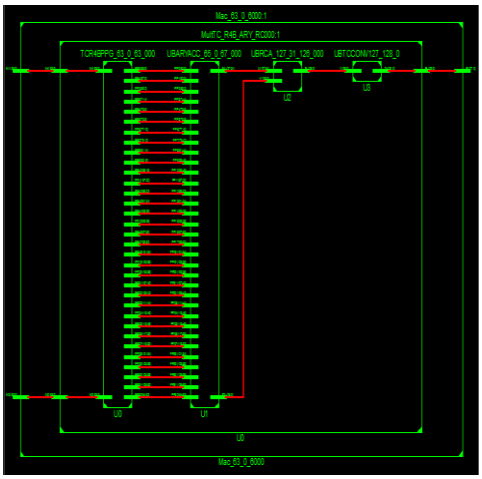
In this paper a new technique is presented under which it is implemented with a powerful mechanism and is shown in the above figure and is explained in an elaborative fashion respectively. Here in the system oriented present implementation based perspective under which it is relative to the strategy of mainly the operation standards are restricted to the unit of the design of the MAC plays a crucial role for the improvement in the performance where there is a reduction of the dissipation of the power based constraints followed by the scenario of the delay based parameters is a major concern respectively. Here this particular thing of the unit of the MAC is integrated and implemented with respect to the strategy of the application of the processing of the signal based on the digital basis and also the applications relative to the multimedia is a major concern and plays crucial role in a well effective manner respectively [4]. Here the design based consideration of the unit of the MAC protocol is done by the help of the accumulator adder and followed by the multiplier is a major concern respectively. Here there is a complete transformation takes place in the system in terms of the entire modification of the system in terms of the improvement in the system there is a new design based strategy is in to the system which includes the specification of the standards of the Wallace based transformation is a major concern respectively. That too it is implemented under the data bits of the 64 bits based strategy in a well effective manner [5][6].

3. EXPECTED RESULTS:

RTL SCHEMATIC



INTERNAL STRUCTURE OF RTL SCHEMATIC



DESIGN SUMMARY

Mac_63_0_6000 Project Status (07/12/2014 - 12:21:50)			
Project File:	mac_64.xise	**Parser Errors:**	No Errors
Module Name:	Mac_63_0_6000	**Implementation State:**	Synthesized
Target Device:	xc3s500e-4fg320	**• Errors:**	No Errors
Product Version:	ISE 13.2	**• Warnings:**	92 Warnings (0 new)
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	4018	4656	86%
Number of 4 input LUTs	7047	9312	75%
Number of bonded IOBs	256	232	110%

Timing Summary:

Speed Grade: -4

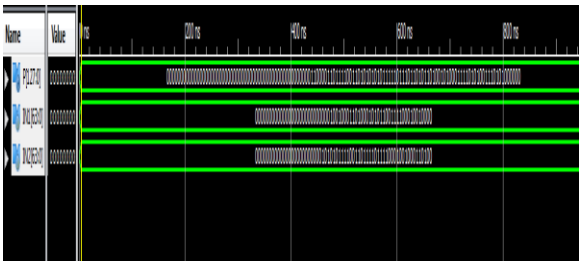
Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 157.269ns

SIMULATION RESULTS



Experiments have been conducted on the present method where the complete analysis of the new method is done and tested in terms of the unknown environments for the further study and the analysis of the present method in terms of the flexibility and also the accuracy plays a crucial role in a well effective manner respectively. Here the complete analysis of the present method that is the Wallace

transform of the modified strategy is shown by the above graphical representation and is explained in a illustrative fashion respectively. Here the design of the present method completely studies the problems of the several previous methods in a well efficient manner under which it completely overcomes the drawbacks of the several previous methods in terms of the improvement in the performance followed by the outcome of the entire system in stipulated fashion respectively. Here the complete analysis of the present method is done with respect to the seve5ral unknown environments with respect to the large number of the datasets in a well efficient manner respectively . Here the complete implementation of the system is done under the specification of the HDL based verilog followed by the standards of the compiler of the RTL based encounter plays a crucial role in its analysis based perspective by the well effective technology of TSMC respectively. Here we finally conclude that the design of the present method is effective and efficient in terms of the improvement in the performance followed by the outcome of the entire system in a well explicit manner respectively.

4. CONCLUSION:

In this paper a new technique is presented under the design oriented strategy of the protocol of the MAC with the standards of the Wallace transformation is a major concern respectively. There is a lot of improvement takes place in the system by the proper integration of the layer of the MAC based protocol in a well effective manner with respect to the design based specification of the Wallace plays a crucial role in its implementation oriented strategy where there is a design of the system takes place under the constraints of the 64 data bits standards in a well crucial manner respectively. Here there is a complete reduction of the dissipation of the power and the delay based constraints is also a major role for the improvement in the performance of the system in a well oriented fashion respectively.

REFERENCES

[1]. Shanthala S, Cyril Prasanna Raj, Dr.S.Y.Kulkarni, "Design and VLST Implementation of Pipelined Multiply Accumulate Unit," IEEE International Conference on Emerging Trends in Engineering and Technology, ICETET-09

[2]. B.Ramkumar, Harish M Kittur and P.Mahesh Kannan, "ASIC Implementation of Modified Faster Carry Save Adder ", European Journal of Scientific Research, Vol. 42, Issue 1, 2010.

[3]. R.UMA, Vidya Vijayan, M. Mohanapriya and Sharon Paul, "Area, Delay and Power Comparison of Adder Topologies",

International Journal of VLSI design & Communication Systems (VLSICSj Vo1.3, No.1, February 2012

[4]. V. G. Oklobdzija, "High-Speed VLSI Arithmetic Units: Adders and Multipliers", in "Design of High-Performance Microprocessor Circuits", Book edited by A.Chandrakasan,IEEE Press,2000

[5]. Dadda, "Some Schemes for Parallel Multipliers," Alta Frequenza, vol. 34, pp. 349-356, 1965

[6]. C.S. Wall ace "A Suggestion for a fast multipliers," IEEE Trans. Electronic Computers, vol. 13, no.l,pp 14-17, Feb. 1967.