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SCHEMING OF VEDIC MATHEMATICS FOR PERFORMANCE INTENSIFICATION OF MULTIPLIER

Shaik Shamsheer Alam[1], Nadella Gopi Nadh[2]

[1]M.Tech Student, Dept of ECE, Nimra Institute of Engineering & Technology, Ongole, A.P, India

[2]Assistant Professor, Dept of ECE, Nimra Institute of Engineering & Technology, Ongole, A.P, India

ABSTRACT:

A multiplier is the essential hardware blocks in the majority of applications for instance digital signal processing encryption as well as decryption algorithms in cryptography. Vedic Sutras pertain to and cover approximately each branch of Mathematics and they concern even to difficult problems relating a great number of mathematical operations. Vedic mathematics has established to be the major tough method for arithmetic operations. Application of Sutras gets better computational skills of learners in an extensive area of problems; ensure speed along with accuracy, severely based on rational as well as consistent reasoning. Application of Sutras accumulates a lot of time as well as attempt in working out problems, when compared to recognized methods currently in vogue. The functioning of an 8-bit Vedic multiplier improved in terms of propagation delay when evaluated with conventional multiplier resembling array multiplier, modified booth multiplier as well as Wallace tree multiplier was described. In the design we have exploited 8-bit barrel shifter which needs simply one clock cycle in support of 'n' number of shifts. Multiplier functioning by means of FPGA has already been reported by means of different multiplier construction but performance of multiplier was enhanced in projected design.

Keywords: Multiplier, Vedic Sutras, Vedic multiplier, Digital signal processing.

1. INTRODUCTION:

Numerous researchers tried to propose multipliers which put forward moreover factors of high speed, low power expenditure, constancy of layout in addition to less area or else even combination of three in multiplier [1]. Multiplier is essential component of applications of digital Signal Processor and therefore speed of processor mostly depends on designing of multiplier. As multiplication dominates implementation time of most digital Signal Processor algorithms, so there is a requirement of high speed multiplier. Presently multiplication time is leading factor in determining instruction cycle time of a digital Signal Processor chip. Vedic Mathematics is an earliest system concerning math practiced at some point in Vedic age which was reconstructed later and was the most refined and proficient mathematical system achievable. One of such resourceful method has been employed to improve design of a multiplier. Vedic mathematics has established to be the major tough method for arithmetic operations. Conventional techniques in support of multiplication make available important amount of delay in hardware functioning of n-bit multiplier [2][3]. The combinational setback of design degrades performance of multiplier. We have applied a high speed Vedic multiplier by means of barrel shifter. The sutra was put into practice by modified plan of Nikhilam Sutra due to its trait of lessening of number of partial products. The barrel shifter which was used at various levels of design severely reduces delay when evaluated to conventional multipliers. The hardware functioning of Vedic multiplier by means of barrel shifter put in to sufficient development of speed in order to attain high outturn.

2. METHODOLOGY:

The functioning of an 8-bit Vedic multiplier improved in terms of propagation delay when evaluated with conventional multiplier resembling array multiplier, modified booth multiplier as well as Wallace tree multiplier was described. In the design we have exploited 8-bit barrel shifter which needs simply one clock cycle in support of ‘n’ number of shifts. The design is put into practice and confirmed by means of FPGA along with ISE Simulator. Vedic Sutras pertain to and cover approximately each branch of Mathematics and they concern even to difficult problems relating a great number of mathematical operations.

Application of Sutras accumulates a lot of time as well as attempt in working out problems, when compared to recognized methods currently in vogue. Although the solutions come into view like magic, the application of Sutras is completely logical in addition to reasonable. The working out made on computers follows, in a means, principles underlying Sutras. The Sutras make available not simply methods of calculation, however also ways of thinking in support of their application. Application of Sutras gets better computational skills of learners in an extensive area of problems; ensure speed along with accuracy, severely based on rational as well as consistent reasoning. Application of Sutras to detailed problems involves realistic thinking, which, in progression helps get better intuition explicitly bottom line of mastery of mathematical geniuses of earlier period and present [3]. Multiplier functioning by means of FPGA has already been reported by means of different multiplier construction but performance of multiplier was enhanced in projected design. The performance of projected multiplier is compared with earlier implemented multipliers on FPGA [4]. In our design, efforts were made to decrease propagation delay as well as achieved development in decrease of delay when evaluated to array multiplier, along with conventional Vedic multiplier functioning on FPGA. The high speed functioning of such a multiplier has extensive range of applications in arithmetic logic unit as well as VLSI signal processing.

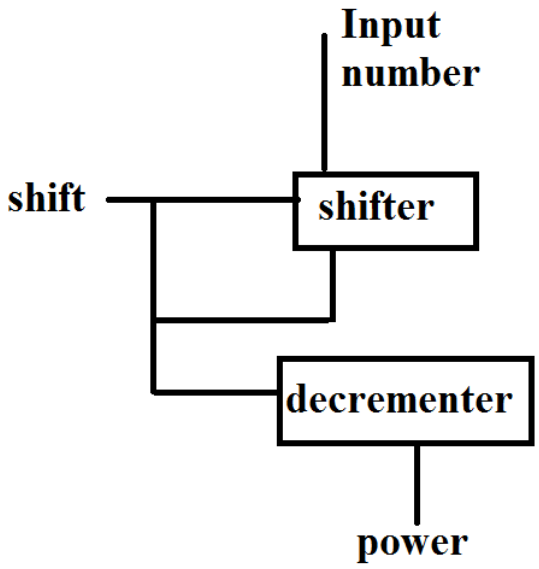


Fig1: An overview of Power Index Determinant

3. ANOVERVIEW OF PROJECTED MULTIPLIER DESIGN:

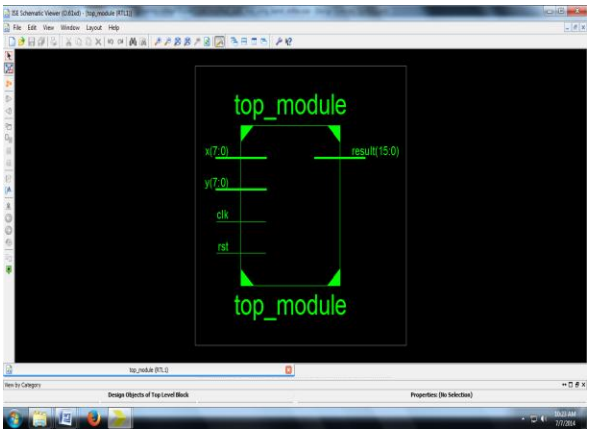
A multiplier is the essential hardware blocks in the majority of applications for instance digital signal processing encryption as well as decryption algorithms in cryptography. Considering multiplier is 'A' and multiplicand is 'B'.

P=A*B= (2^a2)*(A+Z2*2^(a1-a2))+Z1*Z2.

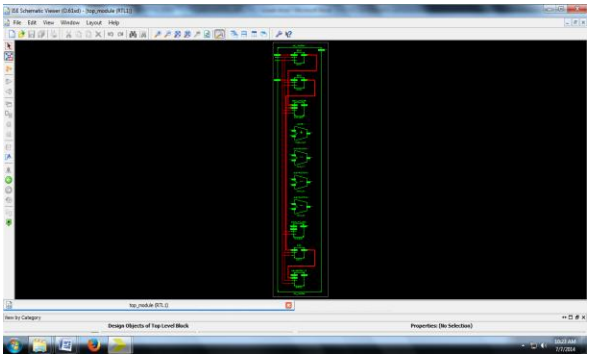
a1, a2 are highest power index of input numbers A and B. Z1 and Z2 are residues in numbers A and B. The hardware exploitation of above expression is separated into three blocks such as Base Selection Module, module of Power index Determinant along with Multiplier. The base selection module is employed to choose greatest base regarding input numbers. The base selection component has power index determinant as sub-module all along with barrel shifter, average determinant, comparator, adder, as well as multiplexer. The power index determinant is employed to remove power index of a1 and a2. The multiplier contains base selection module, power index determinant, adder/subtractor subtractor, barrel shifter, as sub-modules in building. The input number is fed to shifter which will reallocate input bits by means of one clock cycle [5]. In this power index determinant sequential searching has been utilized to look for for first '1' in input number opening from MSB. If search bit is '0' subsequently counter value will decrement up to recognition of input search bit is '1'. Output of decrementer is necessary power index of input number. The base selection along with power index determinant forms integral part of multiplier building. The construction computes mathematical expression in the above given equation. Barrel shifter was used in the construction. The two input numbers are fed towards module of base selection from which base is gained. Outputs of base selection module along with input numbers 'A' and 'B' are fed towards subtractors [6]. The inputs towards power index determinant are from the module of base selection of particular input numbers. The sub-section concerning power index determinant as shown on fig1 is employed to take out power of base and followed by means of subtractor to work out value. The outputs of subtractor are fed towards multiplier that feed the input towards second adder or else subtractor. Similarly outputs concerning power index determinant are fed towards third subtractor that feed input towards barrel shifter.

Simulation results

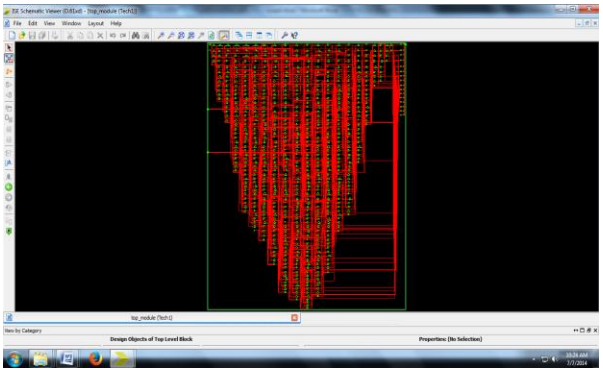
RTL SCHEMATIC



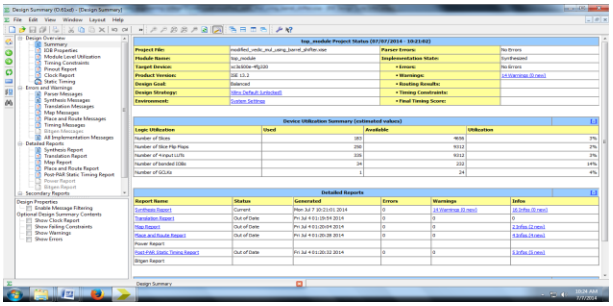
INTERNAL STRUCTURE OF RTL SCHEMATIC



INTERNAL STRUCTURE OF TECHNOLOGY SCHEMATIC



DESIGN SUMMARY



Timing Summary:

Speed Grade: -4

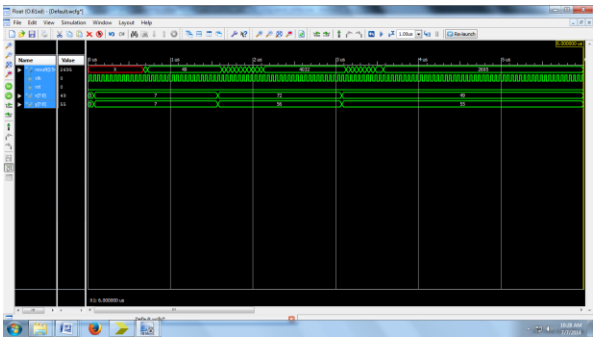
Minimum period: 9.539ns (Maximum Frequency: 104.833MHz)

Minimum input arrival time before clock: 10.287ns

Maximum output required time after clock: 7.676ns

Maximum combinational path delay: No path found

Simulation Results



4. CONCLUSION:

Multiplier is essential component of applications of digital Signal Processor and therefore speed of processor mostly depends on designing of multiplier. Conventional techniques in support of multiplication make available important amount of delay in hardware functioning of n-bit multiplier. Vedic mathematics is an earliest system concerning math practiced at some point in Vedic age which was reconstructed later and was the most refined and proficient mathematical system achievable. The functioning of an 8-bit Vedic multiplier improved in terms of propagation delay when evaluated with conventional multiplier resembling array multiplier, modified booth multiplier as well as Wallace tree multiplier was described. In the design we have exploited 8-bit barrel shifter which needs simply one clock cycle in support of 'n' number of shifts. In our design, efforts were made to decrease propagation delay as well as achieved development in decrease of delay when evaluated to array multiplier, along with conventional Vedic multiplier functioning on FPGA. We have applied a high speed Vedic multiplier by means of barrel shifter. The sutra was put into practice by modified plan of Nikhilam Sutra due to its trait of lessening of number of partial products. The barrel shifter which was used at various levels of design severely reduces delay when evaluated to conventional multipliers. The hardware functioning of Vedic multiplier by means of barrel shifter put in to sufficient development of speed in order to attain high outturn. The high speed functioning of such a multiplier has extensive range of applications in arithmetic logic unit as well as VLSI signal processing.

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