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DESIGN OF VITERBI DECODER UNDER OPTIMIZATION OF THE SPEED BASED ON FPGA

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ABSTRACT:

In terms of the modern philosophy under which there is a effective utilization of the technology relative to the standards of the VLSI plays a crucial role in its implication where there is a reduction of the power based constraints and the reduction of the area based specification and the improvement in the speed based parameters plays a crucial role in its implication followed by the strategy of the data based encoding and the decoding under which relative to the communication standards of the electronics is a major concern respectively. Under the communication based parameters of the wireless environments where there is a huge relativeness by the parameters of the survival path in relation to the design based specification of the viterbi based decoder is a major concern and plays a crucial role for the reduction of the cost followed by the power based specification and in effective to the standards of the improvement in the area is a major concern. Here a new technique is proposed under which it must satisfy the following objectives under the statistics of the design based parameters which includes as follows primarily it includes the scenario of the design of the decoder based on the orthodox viterbi plays a major role and it supposed to be design and then after simulated in a well effective manner. Secondly design of the decoder by the effective improvement in the speed of the system in terms of the input logic oriented diffused gate plays a crucial role in its applicability followed by the well effective strategy of the analysis based perspective using the XILINX software for the effective simulation purpose. There is a comparison of the viterbi based GDIL in effective to the unit of the survival

path of the present system oriented standard that is a previous method in order to evaluate the accuracy of the system based implications respectively. Finally The comparison of the all the decoders of the viterbi in effective to the simulation followed by the synthesis plays a crucial role in a well effective manner respectively. Simulations have been conducted on the present method where there is a lot of analysis takes place in the system under which a test bed is conducted with a large number of the datasets in an unknown environment for the accurate analysis or even testing of the datasets in a well efficient fashion respectively.

KEYWORDS: Decoder of the Viterbi, Optimization of the speed, Modified FPGA (field programmable gate array), Unit of the branch metric, Unit of the compare select adder, Unit of the trace back strategy, XILINX, Technique of GDIL, Back trace, Select compare add, DRAM respectively.

1. INTRODUCTION:

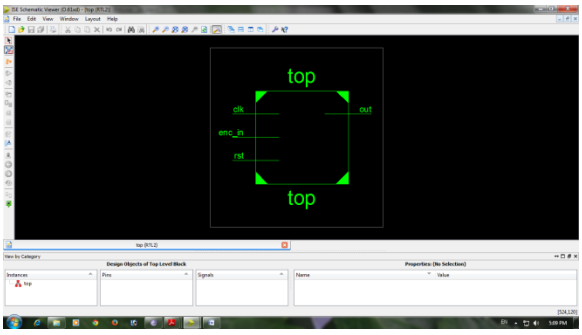
There is a lot of advancement takes place in the system in terms of the decoding algorithm relative to the design of the standards under the specification of the viterbi plays a crucial role in its analysis based perspective is a major concern respectively [1]. Here this particular strategy is implemented in the design of the system relative to the aspect of the communication under which it plays a crucial role for the encounter of the problems relative to the host applications based strategy respectively. Here the sequence of the state transition is from the state space diagram for the well effective implementation of the viterbi plays a role in its analysis based perspective. Here the generation of the data in the form of the sequence plays a crucial role in terms of the noise less basis is a primary concern respectively [2][3]. Here the design of the decoder based on the standards of the viterbi is implemented by the well effective classification of the unit of the branch metric, unit of the compare select followed by the unit of the back trace is a major concern respectively. Here the unit of the branch metric is done by the help of the pythogorous theorem or simply under the design based metric calculation of the Euclidean distance in a well similar fashion respectively.

2. METHODOLOGY:

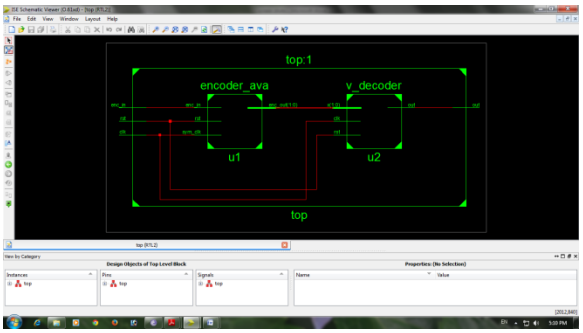
In this paper a new technique is proposed under which it is implemented by the help of the powerful mechanism and is shown by the help of the above figure and is explained in an elaborative fashion respectively. Here the technique of the GDIL is came into the existence under the design of the circuit with the low power based aspect in effective to the reduction of the consumption of the power plays a crucial role in its strategy respectively. Here the acronym of the GDIL is explained as the strategy of the input logic of the gate diffusion respectively. Here the inverter of the complementary metal oxide semi conductor is analogous to that of the cell based on the GDIL plays a crucial role in its applicability based perspective respectively. Here the inputs of the cell based GDIL consists of the three in number followed by the Here there is an interconnection of the PMOS followed by the NMOS that is both (P type and followed by the N type metal oxide semi conductor) respectively. With both junctions of the p type and as well as the n type in a well oriented fashion respectively. There are four terminals included for the standards of the GDIL and which includes the Gate, Diffusion, p and n terminals in a well effective manner respectively [4]. Here the implementation of the GDIL plays a crucial role for the process of the complex data and that too in the simplified fashion respectively. Therefore these are the design parameters of the GDIL system under which that is implemented for the purpose of the reduction of the consumption of the power followed by the reduction of the dissipation of the strategy of the power based constraints and also the well effective area based reduction and that too reduction of the reduction of the noise plays a crucial role and is a major concern respectively [5][6].

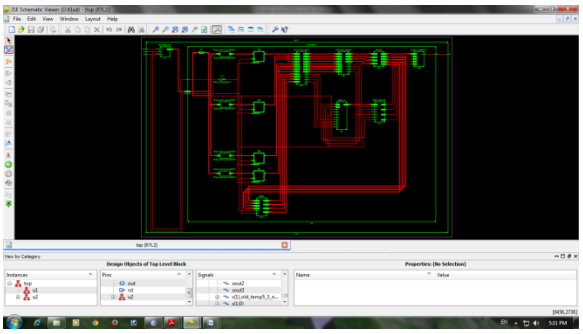
3. EXPECTED RESULTS:

Rtl schematic

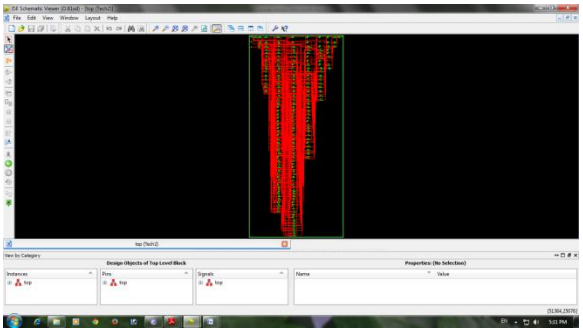


Internal structure of rtl schematic

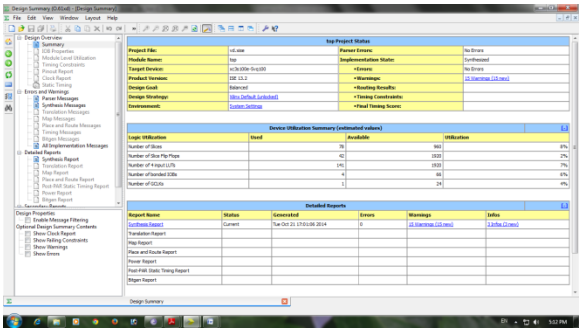




Internal structure of technology schematic



Design summary



Timing Summary:

Speed Grade: -5

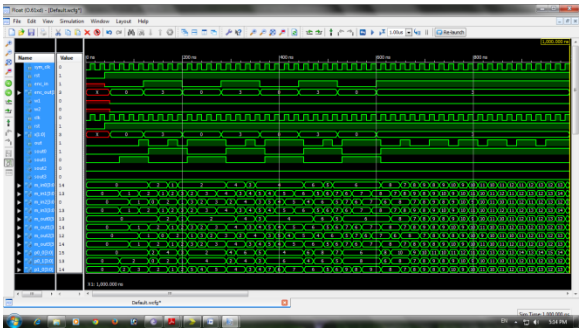
Minimum period: 5.618ns (Maximum Frequency: 177.995MHz)

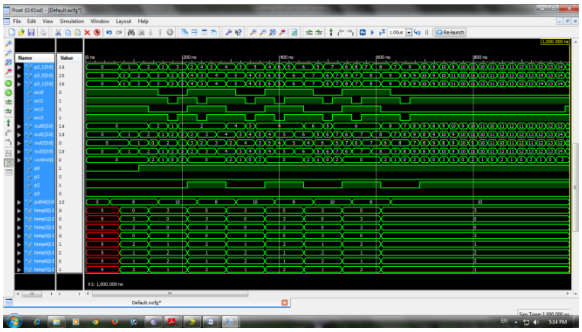
Minimum input arrival time before clock: 2.676ns

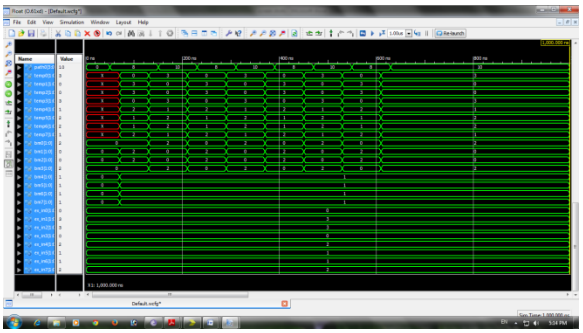
Maximum output required time after clock: 5.536ns

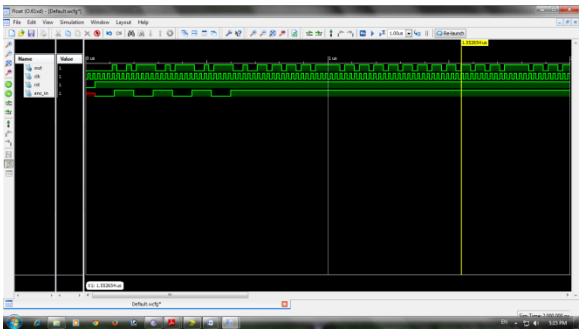
Maximum combinational path delay: No path found

Simulation results









Here the implementation of the present method completely overcomes the drawbacks of the several previous methods in a well effective fashion respectively. Here the design of the present method completely analyzes the problems of the several previous methods in an accurate basis under which it completely studies the problems of the previous methods and it controls the errors in the design of the present method under which there is a rapid improvement in the performance followed by the outcome of the entire system in a well stipulated fashion respectively. Here the implementation of the present method and the simulated results are shown in the above graphical representation and it evaluates the performance of the present implemented method in a well accurate fashion and in an explicit manner respectively. Here we finally conclude that the design of the present method is effective and efficient in terms of the improvement in the performance followed by the outcome of the entire system in a well oriented manner respectively.

4. CONCLUSION:

In this paper a new technique is proposed with a well efficient powerful mechanism under which there is a reduction of the dissipation of the power based constraints in a well effective manner followed by the reduction of the area and the reduction of the operation frequency plays a major role in its applicability point of view respectively. Here various types of the decoders are designed under which it includes the well effective strategy of the select compare add, unit of the back trace followed by the decoder of the three type lays a crucial role in its applicability perspective respectively. Here the present method is accurate in terms of the implementation point of view respectively.

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